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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,630	01/28/2000	Eric T. Stubbs	303.662US1	2483

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EXAMINER

KIM, KEVIN

ART UNIT PAPER NUMBER

2634

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/493,630

Applicant(s)

STUBBS, ERIC T.

Examiner

Kevin Y Kim

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-13, 24-26, 49 and 50 is/are allowed.
- 6) ☒ Claim(s) 14-17, 19-23, 27-48 and 51-53 is/are rejected.
- 7) ☒ Claim(s) 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01-28-2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 37 is rejected under 35 U.S.C. 102(b) as being anticipated by Tsai et al (5,691,669).

Referring to Fig. 1, Tsai et al discloses a variable delay line (140) and a phase detector (120), shown in detail in Figs. 7 and 8 respectively. The variable delay has an input node (IN), an output node (OUT), a fine adjustment input node (710) and a coarse adjustment node (740). The phase detector generates signals to the adjustment nodes.

3. Claim 14-17,19-23,27-48,51-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Jefferson et al (US 5,744,991).

Consider claims 14 and 20. Jefferson et al discloses a memory device for aligning a clock signal to data signals, *see col.1, lines 44-48*, comprising the step of receiving an external clock signal (REFCLK), delaying the signal in a variable delay line (212,216) to produce an internal clock signal (CLKOUT). The variable delay is changed by a first delay amount (Macro delay) when the phase difference is above a threshold and by a second smaller delay when it is below the threshold. Though not described explicitly, the patent appears to cover various known alternatives to providing coarse and fine delays. One would be that the delay time/amount of the variable micro delay (216) is shorter than that of the variable macro. As an alternative, in the

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case of the coarse delay, the input signal is made to go through more delay devices than in the case of the fine delay while the same delay cells are used.

Regarding claims 15 and 16, the internal clock signal (CLKOUT) is used to derive various parts devices and drivers. See col.4, lines 36-43 and col.5, lines 21-31 in particular.

Regarding claim 17, see Lumped delay (214) that delays the internal clock signal before comparing it with the external signal.

Regarding claim 19, the locking requires that the internal clock be delayed by an integer number of the period of the input signal.

Regarding claim 21, see the IDLE control signal from the phase detector (202,218) when the phase difference is below a second threshold such that the amount of delay is not changed.

Regarding claims 22 and 23, as an alternative to providing coarse and fine delays, the input signal is made to go through more delay units in the case of the coarse delay than in the case of the fine delay while the same unit delay cells are used. I.e., multiple delays units are activated in the coarse delay line while a less number of delay units are activated in the fine delay line.

Consider claims 34,51. Jefferson et al discloses a variable delay line comprising: "a coarse adjustment portion" comprising "a first plurality of delay cells" (212) and "a first shift register" (212), and "a fine adjustment portion" comprising "a second plurality of delay cells" (216) and "a second shift register" (220). See col.8, lines 54-60. As mentioned above the patent covers various known alternatives to implement coarse and fine delays. One would be that the delay time of the variable micro delay (216) is shorter than that of the variable macro. An alternative, in the case of the coarse delay, the input signal is made to go through more delay

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devices than in the case of the fine delay while the same delay cells are used. Additionally regarding claim 51, Jefferson et al discloses a processor and a memory having a delay locked loop. See Fig.1A, and col.1, lines 44-48.

Regarding claims 35 and 52, the first shift register (210) is responsive to a phase detector (202).

Regarding claim 36 and 53, the second shift register (220) is responsive to a phase detector (218).

Consider claim 37, Jefferson et al discloses "a variable delay line" (212, 216) having an input node (213), an output node (217), a fine adjustment node (219) and a coarse adjustment node (21). A phase detector (202, 218) is also disclosed driving signals onto the fine and coarse adjustments nodes.

Regarding claims 38 and 39, Up/Right and Down/Left control signals to the shift register/counter read on increase and decrease adjustment nodes, respectively.

Regarding claims 40-42, the clock output (CLKOUT) is connected to the enable input or clock input of any driver. See col.4, lines 36-43 and col.5, lines 21-31 in particular.

Regarding claims 43-45, see col.1, lines 44-48, teaching the DLL of Jefferson et al is used in memories, ASIC and microprocessor among other things.

Consider claims 27 and 46. Jefferson et al discloses a processor and a memory having a delay locked loop. See Fig.1A, and col.1, lines 44-48 teaching the DLL is used in memories. The DLL comprises a variable delay line including a plurality of delay cells (212,216), a shift register having a plurality of blocks (210, 220) of storage elements corresponding to the delay

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cells. A phase detector (202, 218) is also disclosed to have fine and coarse adjustments nodes (208, 222).

Regarding claims 28,29, 47, the shift register (210,220) shifts the shifter register (210) in response to an asserted signal (Left/Right/Idle).

Regarding claims 30,48, the variable delay line includes an input node (211) and an output node (217), and the phase detector measures a phase difference between an input signal and (REFCLK) and an output (221) of the variable delay line.

Regarding claim 31, see col.8, lines 1-16, where it is taught that the phase detector asserts a coarse control signal when the phase difference is above a threshold and a fine control signal when it is below the threshold.

Regarding claims 32 and 33, though not described explicitly, it is inferred that the delay value of the variable micro delay (216) is smaller than that of the variable macro delay (212) since the function of the variable micro delay (216) is to further adjust the delayed clock from the variable macro delay (212) in a finer step.

Allowable Subject Matter

4. Claims 1-13,24-26,49-50 are allowed.
5. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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6. The following is a statement of reasons for the indication of allowable subject matter: No prior art has been found to teach a delay locked loop where the phase difference between an input signal and a feedback signal and the phase difference between a delayed input signal and the feedback signal are used to adjust the phase of the input signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


Arai (US 6,259,330), Ketzler (US 4,714,924), Casasanta et al (US 5,844,954), Tsai et al (US 5,691,669) each teach coarse and fine delay.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y Kim whose telephone number is 703-305-4082. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

kvk
June 12, 2003


STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
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